REMARKS

Claims 1-16 and 18 are pending in this application, of which claims 1-15 have been withdrawn, and claim 16 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention.

Claim Rejections under 35 USC §112

Claims 16 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Specifically, the Examiner asserts that claims 16 and 18 recite that the total thickness of the first and second silicon films are substantially equal to the total thickness of the third and second silicon films. The Examiner further asserts that this implies that thickness of the first and third silicon films are substantially equal and it is this limitation that does not have support in the specification.

Applicants disagree with the Examiner, however have, nevertheless, amended claim 16 to cancel this feature of the invention.

Therefore, withdrawal of the rejection of Claims 16 and 18 under 35 U.S.C. 112, first paragraph, is respectfully requested.

Claim Rejections under 35 USC §103

Claims 16 and 18 are rejected under 35 USC §103(a) as being unpatentable over admitted Prior Art Figures 8 and Gwen et al. (U.S. Patent No. 5,472,892).

Figure 8 describes an integrated circuit in the prior art having a flash memory (A), a low voltage transistor (B), and mid-level voltage transistor (D), and a high voltage transistor (C). A semiconductor substrate is used as the base for each of the foregoing devices. In addition, insulation (12B) is shown with a thickness of 1.5-5 nm, insulation (12D) is shown with a thickness of 5-10 nm, and insulation (12C) has a thickness of 8-50 nm. In addition, gate electrode (16), as solely illustrated by figure 8J, appears to illustrate electrodes 16 of equal height. A floating gate (13) with a control gate (16) is formed on the silicon gate (13) using an ONO film (14), as shown in figure 8B. It should also be noted that silicon gate (13) is also referred to as a floating gate (13) in the discussion of figure 17.

Gwen et al. describes the method of the manufacturing gate memory in which a silicon layer (206) is placed in a cell array region and a silicon layer (208) is placed in a peripheral circuit region. According to figure 3I, silicon layer (208) appears to be placed directly upon silicon layer (206).

Claims 16 and 18 are objected to as reciting product by process claims. The applicant disagrees with the Examiner's assertions, current claims 16 and 18 recite a device structure.

Although the gate electrode is formed by stacking of two polysilicon layers, the boundary of these two polysilicon layers are generally observable by electron microscopic observation.

Amended claim 16 recites the feature that a silicide film is stacked directly on the first silicon film in the first and third gate electrodes and that the silicide film is stacked directly on the third silicon film in the second gate electrode. The support of use of silicide film for the film 21 is given at page 42, line 7 of the original disclosure.

According to the present invention, it becomes possible to achieve the same height for the entire first through third gate electrodes by choosing the thickness of the first and third silicon films and the silicide film appropriately. Such a structure is clearly distinguished from the structure of Figure 8 of the Admitted Prior Art.

Contrary to the present invention as set forth in claim 16, Gwen merely teaches lamination of two polysilicon layers separated from each other by an insulation film. Further, in Gwen, there is no teaching of achieving the same height for different gate. Thus, even if Gwen is combined with the Admitted Prior Art, the subject matter of claim 16 would not be derived.

Therefore, amended claim 16 patentably distinguishes over the prior art relied upon by reciting,

> "A semiconductor integrated circuit, comprising: a semiconductor substrate; a non-volatile memory formed in a memory cell region of said semiconductor substrate; a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode; a second MOS transistor formed on a second device region of said semiconductor substrate, said

> second MOS transistor having a second gate oxide film of second thickness and a second gate electrode; and a third MOS transistor formed on a third device region of said semiconductor substrate, said third MOS transistor having a third gate insulation film of third thickness and a third gate electrode; said first thickness being smaller than said second thickness, said second thickness being smaller than said third thickness, wherein said first and third gate electrodes have a structure in which a silicide film is formed directly on a first silicon film, said second gate electrode has a structure in which said silicide film is formed directly on a third silicon film, and wherein said non-volatile memory is formed of a floating gate electrode formed of said third silicon film and a control gate electrode formed on said floating gate electrode via an insulation film and having a structure in which said first silicon film and said second silicon film are consecutively stacked." (Emphasis Added)

Therefore, withdrawal of the rejection of Claims 16 and 18 under 35 USC §103(a) as being unpatentable over admitted Prior Art Figures 8 and Gwen et al. (U.S. Patent No. 5,472,892) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 16 and 18 are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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